UWB RADAR SENSOR IC
[SR-RUG0-083C-01 Datasheet]

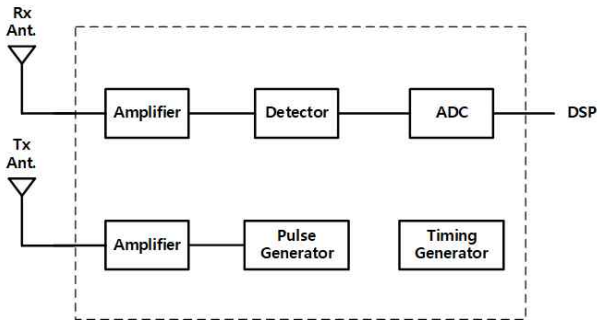
Key Features

- Fully Integrated Impulse UWB Radar IC
- Integrated Analog to Digital Converter(ADC)
- 7 - 9 GHz UWB high-band operating frequency
- Tunable Bandwidth 500MHz ~ 1.4GHz
- Detection Range: ~ 15.0m (max. available)
- Power down(save) mode
- Operating Temperature: -20 to +85˚C
- External Tx/Rx mode control
- CMOS compatible I/O
- RF CMOS technology with ESD protection
- SPI interface
- Low power consumption
- 48 Lead 7x7 mm QFN Package: 49mm^2

Application

- Motion Detection
- Presence Detection
- Security Sensors
- Collision Avoidance
- People Counting

Block Diagram



Packaged IC [48 Lead QFN 7X7mm]

General Description

The SR-RUG0-083C-01 is a fully integrated impulse UWB radar IC that detects objects up to Max. 15.0m.

This IC can be used for applications such as parking lot detection, collision prevention, and human recognition.

The frequency is 7.0 ~ 9.0GHz high-band operating frequency, and the 10dB bandwidth is variable from 0.5 ~ 1.4GHz.

In order to implement the low power consumption, the power down (save) mode is selectively applied and ESD protection technology is applied. The package used was a 48 lead 7x7 mm QFN package.

UWB RADAR SENSOR IC
[SR-RUG0-083C-01 Datasheet]

UWB Radar IC Specification

Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{ST}	- 20	-	+ 85	°C
Supply Voltage	$V_{DD}1$		1.2		V
	$V_{DD}2$		3.3		V

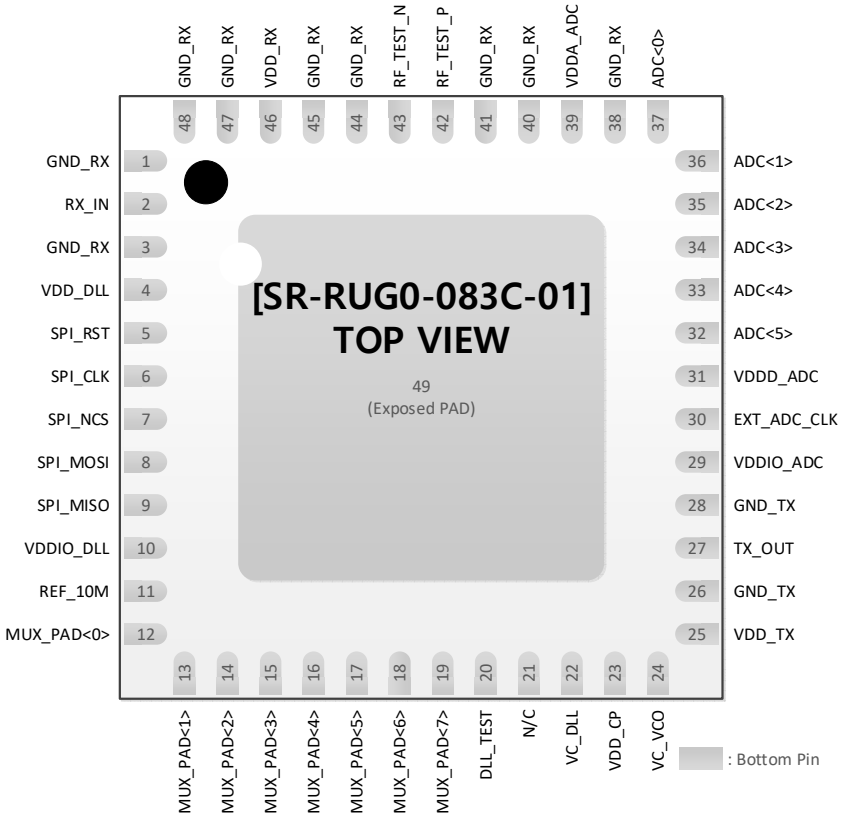
Electrical Specification

Parameter	Min	Typ	Max	Unit	Descript.
Frequency Range (carrier)	7		9	GHz	Carrier tunable
Bandwidth	0.5		1.4	GHz	BW tunable
EIRP (Effective Isotropic Radiated Power)		-43.3	-41.3	dBm	Average power @ 1MHz RBW
		-37.0	-24.4		Peak power @3MHz RBW
Rx Gain Control Dynamic Range	20		66	dB	
Sampling Rate		2		Gbps	
Detection Range	0.5		15	m	
Detection Resolution		7.5		cm	
PRF (Pulse Repetition Rate)		10		MHz	External 10MHz X-tal. needed
ADC resolution		6		Bits	
Current consumption(1)		120		mA	@ +1.2V, duty 100%
		5		mA	@ +3.3V, duty 100%

(1) Power consumption at full operation is 120mA. However, in most applications, 1 or 10% duty is satisfactory for detection and tracking. The power can be reduced significantly by low duty and power down function.

PIN Description

- Pin out(Top view)



- Pin definition and function

PIN No.	Pin Name	I/O	Description
1	GND_RX	-	Ground for RX area
2	RX_IN	I	Received RF signal Input
3	GND_RX	-	Ground for RX area
4	VDD_DLL	I	VDD +1.2V for DLL
5	SPI_RST	I	SPI Reset
6	SPI_CLK	I	SPI Clock
7	SPI_NCS	I	SPI Chip selection
8	SPI_MOSI	I	SPI Master output slave input
9	SPI_MISO	O	SPI Master input slave output
10	VDDIO_DLL	I	VDD +3.3V for DLL
11	REF_10M	I	10MHz reference clock signal Input
12-19	MUX_PAD<0:7>	I	External MUX_PAD<0:7> array input
20	DLL_TEST	O	DLL test port. The DLL output waveform can be checked via this pin.

21	SWEEP_START	I	MUX_PAD<0:7> Sweep start input
22	VC_DLL	O	External loop filter for DLL. This pin should be decoupled to the ground plane with a capacitor, typically 10 nF.
23	VDD_CP	I	VDD +1.2V for DLL charge pump
24	VC_VCO	I	Voltage control for TX VCO. The center frequency can be adjusted by adjusting this voltage.
25	VDD_TX	I	VDD +1.2V for TX
26	GND_TX	-	Ground for TX area
27	TX_OUT		RF signal Output Transmitted
28	GND_TX	-	Ground for TX area
29	VDDIO_ADC	I	VDD +3.3V for ADC IO pad
30	EXT_ADC_CLK	I	External clock for ADC. Typically, this pin should be opened.
31	VDDD_ADC	I	VDD +3.3V for ADC digital block
32	ADC<5>	O	ADC output<5> [MSB]
33	ADC<4>	O	ADC output<4>
34	ADC<3>	O	ADC output<3>
35	ADC<2>	O	ADC output<2>
36	ADC<1>	O	ADC output<1>
37	ADC<0>	O	ADC output<0> [LSB]
38	GND_RX	-	Ground for RX area
39	VDDA_ADC	I	VDD +1.2V for ADC analog block
40	GND_RX	-	Ground for RX area
41	BBA_OUTP	O	BBA (+) signal output. This pin can be used to monitor the Base band output signal
42	BBA_OUTN	O	BBA (-) signal output. This pin can be used to monitor the Base band output signal
42	RF_OUTP	O	RF (+) signal output. This pin can be used to monitor the RFRX output signal before down mixer.
43	RF_OUTN	O	RF (-) signal output. This pin can be used to monitor the RFRX output signal before down mixer.
45	GND_RX	-	Ground for RX area
46	VDD_RX	I	VDD +1.2V for RX
47	GND_RX	-	Ground for RX area
48	GND_RX	-	Ground for RX area
49	Exposed PAD	-	This exposed pad must be connected to ground.

- External Tx / Rx mode control
- 10MHz reference clock
- CMOS compatible inputs/outputs
- RF CMOS technology with ESD protection
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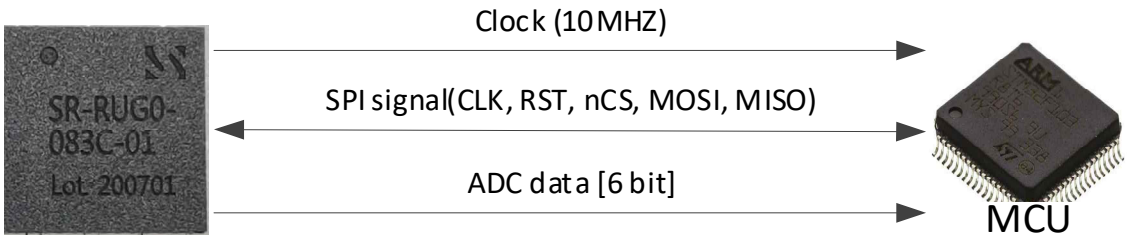
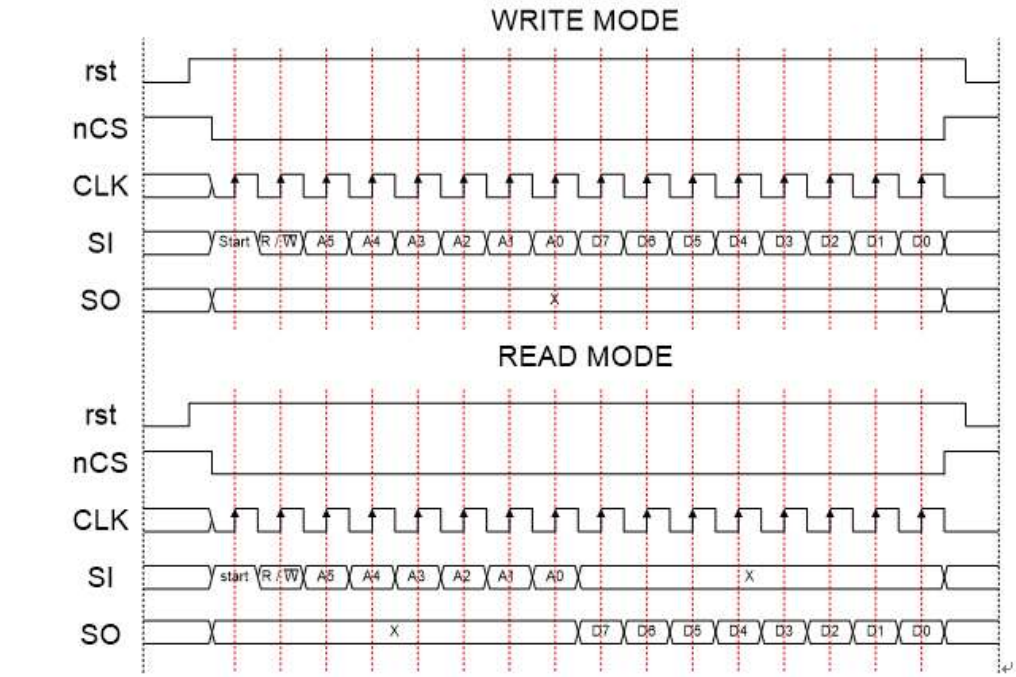
UWB Radar IC and Board Pin connection



Serial Interface Timing Diagram

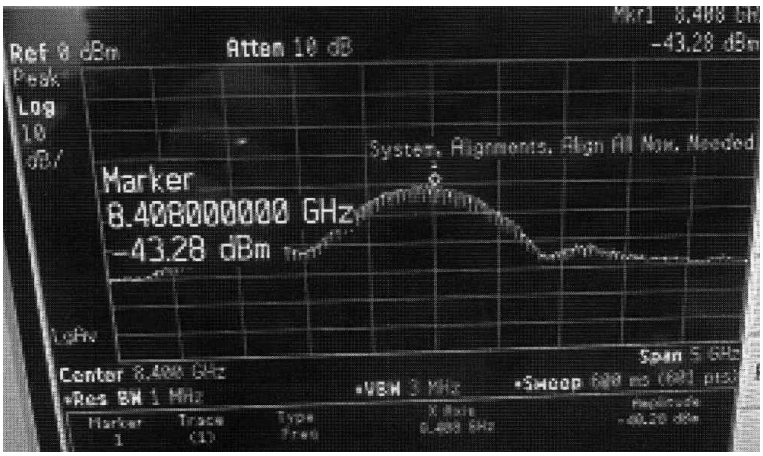


NOTE

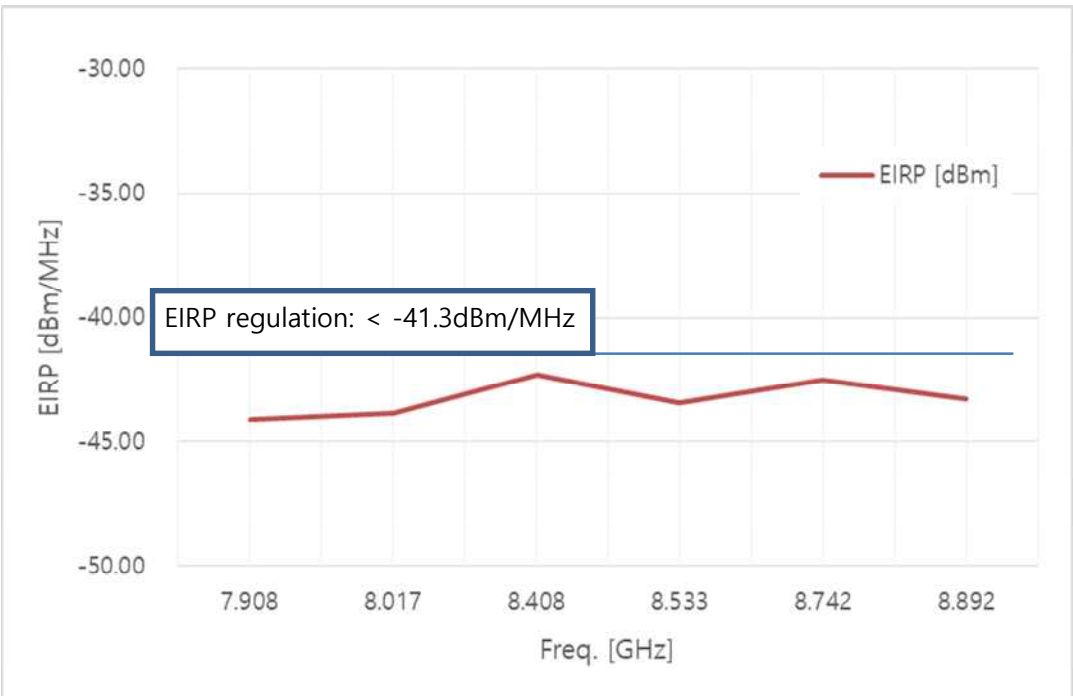
1. Each 8-bit Data and Address signal is received by MSB.
2. When whole register does access or individuation register access everything first time, DFF must receive RST.
3. Data in MCU changes state in CLK's negative edge. So, SPI in chip is sampling data in CLK's positive edge.

Typical Operating Characteristics

- Tx EIRP(@ Avg power) vs. Frequency
  1) EIRP Spectrum(@ Center Frequency)



  2) EIRP vs. Frequency



SPI Register Information

REG00 : Enable_1 (0xF7)

BIT	Name	Default	Description	Status
7	EN_LNA	1	Enable for LNA	Enable 1 Disable 0
6	EN_RFVGA1	1	Enable for RF VGA[Variable Gain Amp.]1	Enable 1 Disable 0
5	EN_RFVGA2	1	Enable for RF VGA2	Enable 1 Disable 0
4	EN_RFVGA3	1	Enable for RF VGA3	Enable 1 Disable 0
3	EN_RF_TEST	0	Enable for RF Test Buffer to monitor Down converter RF input signal	Enable 1 Disable 0
2	EN_MIX	1	Enable for Down converter	Enable 1 Disable 0
1	EN_TIA	1	Enable for TIA	Enable 1 Disable 0
0	EN_TIA_DCOC	1	Enable for TIA DC Offset Cancellation	Enable 1 Disable 0

REG01 : Enable_2 (0xFD)

BIT	Name	Default	Description	Status
7	EN_RFVCM	1	Enable for RF VCM(common mode)	Enable 1 Disable 0
6	EN_BBA	1	Enable for BBA, BBA CORE, DC Offset cancellation When this register is TTL LOW, these functions are turned off at once.	Enable 1 Disable 0
5	EN_BBA_CORE	1	Enable for BBA CORE	Enable 1 Disable 0
4	EN_BBA_DCOC	1	Enable for BBA DC Offset Cancellation	Enable 1 Disable 0
3	EN_BBA_BIAS	1	Enable for BBA Bias	Enable 1 Disable 0
2	EN_BBA_BUFF	1	Enable for BBA Buffer	Enable 1 Disable 0
1	EN_IREF_RX	1	Enable for RX IREF(Current Reference)	Enable 1 Disable 0
0	EN_ITEMP_RX	0	Enable for RX ITEMP (Temperature Compensation Current)	Enable 1 Disable 0

REG02 : Enable_3 (0x38)

BIT	Name	Default	Description	Status
7	EN_BBA_OUT	0	Enable for BBA output switch	Enable 1 Disable 0
6	-	-	Reserved (Recognized as 0)	
5	EN_SH	1	Enable for ADC SAH(sampling and hold) function	Enable 1 Disable 0
4	EN_COMP	1	Enable for ADC comparator	Enable 1 Disable 0
3	EN_VREF	1	Enable for ADC comparator voltage reference generator	Enable 1 Disable 0
2	-	-	Reserved (Recognized as 0)	
1	TIA_DCOC_CTUNE	0	TIA DCOC control(H:361kHz/L:734kHz)	Enable 1 Disable 0
0	BBA_DCOC_CTUNE	0	BBA DCOC control(H:232kHz/L:696kHz)	Enable 1 Disable 0

REG03 : Enable_4 (0xFC)

BIT	Name	Default	Description	Status
7	EN_PFD	1	Enable for DLL phase-frequency detector	Enable 1 Disable 0
6	EN_CP	1	Enable for DLL charge pump	Enable 1 Disable 0
5	EN_MUX	1	Enable for DLL MUX	Enable 1 Disable 0
4	EN_VCDL	1	Enable for DLL voltage-controlled delay line	Enable 1 Disable 0
3	EN_TX_DATA	1	Enable for TX clock buffer	Enable 1 Disable 0
2	EN_ADC_CLK	1	Enable for ADC clock buffer	Enable 1 Disable 0
1	EN_DLL_TEST	0	Enable for DLL test buffer	Enable 1 Disable 0
0	-	-	Reserved (Recognized as 0)	

REG04 : Enable_4 (0x87)

BIT	Name	Default	Description	Status
7	EN_START_UP	1	Enable for DLL start up	Enable 1 Disable 0
6:3	-	-	Reserved (Recognized as 0)	
2	EN_IREF_PG_BIAS	1	Enable for TX pulse generator voltage bias	Enable 1 Disable 0
1	EN_I_BIAS	1	Enable for TX IREF(current reference)	Enable 1 Disable 0
0	EN_VCO	1	Enable for TX VCO	Enable 1 Disable 0

REG05 : Enable_5 (0XF0)

BIT	Name	Default	Description	Status
7	EN_VCO_BUFFER	1	Enable for TX VCO buffer	Enable 1 Disable 0
6	EN_DA_BUFFER	1	Enable for TX driver amplifier buffer	Enable 1 Disable 0
5	EN_LO_BUFFER	1	Enable for TX LO buffer	Enable Disable
4	EN_DA	1	Enable for TX driver amplifier	Enable Disable
3:2	EN_BUFFER_CTRL <1:0>	X0	Enable for TX DA buffer control<1:0> (11:On, 01:Off, X0:Swtiching)	
1:0	EN_PULSE_CTRL<1:0>	X0	Enable for TX DA control<1:0> (11:On, 01:Off, X0:Swtiching)	

REG06 : RF Gain control (0x80)

BIT	Name	Default	Description	Status
7:5	RF_GC_SPI<2:0>	100	Enable for RF Gain Control by SPI<2:0>	0 or 1
4:1	-	-	Reserved (Recognized as 0)	
0	RF_GC_SEL	0	RF gain control select. This bit must be fixed to “0”.	0

RF Gain Control table (These gain values are simulation results.)					
7 to 4 bit Code		Gain [dB]	7 to 4 bit Code		Gain [dB]
BIN.	HEX.		BIN.	HEX.	
1110	E	11	0110	6	28
1100	C	15	0100	4	31
1010	A	20	0010	2	36
1000	8	24	0000	0	40

REG07 : BBA Gain control (0x80)

BIT	Name	Default	Description	Status
7:4	BBA_GC<3:0>	1000	Enable for BBA Gain Control by SPI	0 or 1
3:0	-	-	Reserved (Recognized as 0)	

BBA Gain Control table (These gain values are simulation results.)					
7 to 4 bit Code		Gain [dB]	7 to 4 bit Code		Gain [dB]
BIN.	HEX.		BIN.	HEX.	
0000	00	10	1110	E0	23
0010	20	14	1111	F0	27
0110	60	18	-	-	-

REG08 : ADC operation (0xC0)

BIT	Name	Default	Description	Status
7	CTRL_ADC_SH	1	Enable for Sampling and Hold DC Control	Enable 1 Disable 0
6	CTRL_COMP_VREF	1	Enable for Comparator Voltage Reference Control	Enable 1 Disable 0
5:1	-	-	Reserved (Recognized as 0)	
0	ADC_MUX_SEL	0	ADC MUX Select	PAD 1 DLL 0

REG09 : DLL CONTROL(0x88) [*Don't change these default values.*]

BIT	Name	Default	Description
7:5	CP_BMC<2:0>	100	Charge Pump Binary Mismatch Control<2:0>
4	-	-	Reserved (Recognized as 0)
3:2	PFD_RDC<1:0>	10	Phase-Frequency Detector Reset delay
1	-	-	Reserved (Recognized as 0)
0	PFD_POL	0	Phase-Frequency Detector Polarity

REG10(0A) : Tx MUX mode selection(0x00)

BIT	Name	Default	Description	Status
7:4	-	-	Reserved (Recognized as 0)	
3:2	BIN_SWEEP_SEL TX_SEL_MUX	00	Enable to control by SPI or LOGIC or PAD (11:SPI, 01:LOGIC, X0:PAD)	
1	-	-	Reserved (Recognized as 0)	
0	TX_REF_CLK_SEL	0	TX reference clock selection	External 1 DLL 0

REG11(0B) : Start point for SPI BIN sweep (0x00)

BIT	Name	Default	Description
7:0	BIN_SWEEP_SPI<7:0>	0000 0000	DLL MUX control by SPI Set to start point for SPI BIN sweep

REG12(0C) : Frequency & pulse shape control(0x70)

BIT	Name	Default	Description	Status
7:4	FTRIM<3:0>	0111	TX Center Frequency Control Adjusting these BITs allows center frequency tuning from 7.09~9.56GHz. The values in the table below can be slight different depending on the IC characteristics.	
3	-	-	Reserved (Recognized as 0)	
2:0	PULSE_SW <2:0>	000	TX Sidelobe Rejection Control<2:0> These bits control the sidelobe removal by adjusting the switching shape of the drive amplifier inside the UWB radar sensor IC.	

Center Frequency Control table (These values are test results.)					
7 to 4 bit Code		Frequency [GHz]	7 to 4 bit Code		Frequency [GHz]
BIN.	HEX.		BIN.	HEX.	
1111	F	7.09	0111	7	7.41
1110	E	7.26	0110	6	8.53
1101	D	7.27	0101	5	8.74
1100	C	7.42	0100	4	8.89
1011	B	7.53	0011	3	9.06
1010	A	7.70	0010	2	9.31
1001	9	7.91	0001	1	9.51
1000	8	8.02	0000	0	9.56

REG13(0D): PULSE_A (0xC1)

BIT	Name	Default	Description
7:6	PULSE_A<1:0>	11	Rising edge coarse control for digital pulse generator.
5:3	-	-	Reserved (Recognized as 0)
2:0	PULSE_A_VBIAS<2:0>	001	Rising edge fine control for digital pulse generator.

REG14(0E): PULSE_B (0x01)

BIT	Name	Default	Description
7:6	PULSE_B<1:0>	00	Falling edge coarse control for digital pulse generator.
5:3	-	-	Reserved (Recognized as 0)
2:0	PULSE_B_VBIAS<2:0>	001	Falling edge fine control for digital pulse generator.

REG15(0F): BUFFER Enable (0xC3)

BIT	Name	Default	Description
7:6	BUFFER<1:0>	11	DA buffer enable time coarse control.
5:3	-	-	Reserved (Recognized as 0)
2:0	BUFFER_VBIAS<2:0>	011	DA buffer enable time fine control.

REG16(10): Current control_1 (0x63)

BIT	Name	Default	Description
7:5	IREF_CTRL_LNA_50U<2:0>	011	Current Reference Control for LNA
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_RFVGA1_50U<2:0>	011	Current Reference Control for RF VGA1

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	20
0010	2	0001	1	30
0100	4	0010	2	40
0110	6	0011	3	50
1000	8	0100	4	60
1010	A	0101	5	70
1100	C	0110	6	80
1110	E	0111	7	90

REG17(11): Current control_2 (0x63)

BIT	Name	Default	Description
7:5	IREF_CTRL_ RFVGA 2_50U<2:0>	011	Current Reference Control for RF VGA2
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_RFVGA3_50U<2:0>	011	Current Reference Control for RF VGA3

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	20
0010	2	0001	1	30
0100	4	0010	2	40
0110	6	0011	3	50
1000	8	0100	4	60
1010	A	0101	5	70
1100	C	0110	6	80
1110	E	0111	7	90

REG18(12): Current control_3 (0x00)

BIT	Name	Default	Description
7:5	IREF_CTRL_ LNA_TEMP_50U<2:0>	000	Temperature compensation current control for LNA
4:3	-		Reserved (Recognized as 0)
2:0	IREF_CTRL_RFVGA1_TEMP_50U<2:0 >	000	Temperature compensation current control for RFVGA1

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	20
0010	2	0001	1	30
0100	4	0010	2	40
0110	6	0011	3	50
1000	8	0100	4	60
1010	A	0101	5	70
1100	C	0110	6	80
1110	E	0111	7	90

REG19(13) : Current control_4 (0x00)

BIT	Name	Default	Description
7:5	IREF_CTRL_RFVGA2_TEMP_50U<2:0>	000	Temperature compensation current control for RFVGA2
4:3	-		Reserved (Recognized as 0)
2:0	IREF_CTRL_RFVGA3_TEMP_50U<2:0>	000	Temperature compensation current control for RFVGA3

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	20
0010	2	0001	1	30
0100	4	0010	2	40
0110	6	0011	3	50
1000	8	0100	4	60
1010	A	0101	5	70
1100	C	0110	6	80
1110	E	0111	7	90

REG20(14): Current control_5 (0x03)

BIT	Name	Default	Description
7:5	IREF_CTRL_RF_TEST_50U<2:0>	000	Current Reference Control for RF TEST
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_MIX_50U<2:0>	011	Current Reference Control for RX mixer

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	20
0010	2	0001	1	30
0100	4	0010	2	40
0110	6	0011	3	50
1000	8	0100	4	60
1010	A	0101	5	70
1100	C	0110	6	80
1110	E	0111	7	90

REG21(15): Current control_6 (0x63)

BIT	Name	Default	Description
7:5	IREF_CTRL_TIA_50U<2:0>	011	Current Reference Control for TIA
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_ADC_CLK_BUFFER _50U<2:0>	011	Current Reference Control for ADC clock buffer

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	20
0010	2	0001	1	30
0100	4	0010	2	40
0110	6	0011	3	50
1000	8	0100	4	60
1010	A	0101	5	70
1100	C	0110	6	80
1110	E	0111	7	90

REG22(16): Current control_7 (0x63)

BIT	Name	Default	Description
7:5	IREF_CTRL_DLL_CLK_BUFFER _50U<2:0>	011	Current Reference Control for DLL clock buffer
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_DLL_CP_50U<2:0>	011	Current Reference Control for DLL Charge Pump

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	20
0010	2	0001	1	30
0100	4	0010	2	40
0110	6	0011	3	50
1000	8	0100	4	60
1010	A	0101	5	70
1100	C	0110	6	80
1110	E	0111	7	90

REG23(17): Current control_8 (0X00)

BIT	Name	Default	Description
7:5	IREF_CTRL_MIX_TEMP_50U<2:0>	000	Temperature compensation current control for Down convertor
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_TIA_TEMP_50U<2:0>	000	Temperature compensation current control for TIA

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	20
0010	2	0001	1	30
0100	4	0010	2	40
0110	6	0011	3	50
1000	8	0100	4	60
1010	A	0101	5	70
1100	C	0110	6	80
1110	E	0111	7	90

REG24(18): Current control_9 (0x63)

BIT	Name	Default	Description
7:5	IREF_CTRL_TIA_DCOC_20U<2:0>	011	Current Reference Control for TIA DCOC
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_RFVCM_20U<2:0>	011	Current Reference Control for RF VCM

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	8
0010	2	0001	1	12
0100	4	0010	2	16
0110	6	0011	3	20
1000	8	0100	4	24
1010	A	0101	5	28
1100	C	0110	6	32
1110	E	0111	7	36

REG25(19): Current control_10 (0x60)

BIT	Name	Default	Description
7:5	IREF_CTRL_BBA_20U<2:0>	011	Current Reference Control for BBA
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_TEMP_20U<2:0>	000	Current Reference Control for Temperature Sensor

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	8
0010	2	0001	1	12
0100	4	0010	2	16
0110	6	0011	3	20
1000	8	0100	4	24
1010	A	0101	5	28
1100	C	0110	6	32
1110	E	0111	7	36

REG26(1A): Current control_11 (0xE7)

BIT	Name	Default	Description
7:5	IREF_CTRL_ADC_SH_20U<2:0>	111	Current Reference Control for ADC sampling and hold
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_ADC_COMP_20U<2:0>	111	Current Reference Control for ADC comparator

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	8
0010	2	0001	1	12
0100	4	0010	2	16
0110	6	0011	3	20
1000	8	0100	4	24
1010	A	0101	5	28
1100	C	0110	6	32
1110	E	0111	7	36

REG27(1B): Current control_12 (0x00)

BIT	Name	Default	Description
7:5	IREF_CTRL_DUM1_20U<2:0>	000	Control for 20uA current reference main unit. Set the unused control to “0” in the “main unit”.
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_DUM2_20U<2:0>	000	Control for 20uA current reference main unit. Set the unused control to “0” in the “main unit”.

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	8
0010	2	0001	1	12
0100	4	0010	2	16
0110	6	0011	3	20
1000	8	0100	4	24
1010	A	0101	5	28
1100	C	0110	6	32
1110	E	0111	7	36

REG28(1C): Current control_13 (0x63)

BIT	Name	Default	Description
7:5	IREF_CTRL_TX_50U<2:0>	011	Current Reference Control for TX Pulse generator bias
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_BUFFER_50U<2:0>	011	Current Reference Control for TX DA buffer

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	20
0010	2	0001	1	30
0100	4	0010	2	40
0110	6	0011	3	50
1000	8	0100	4	60
1010	A	0101	5	70
1100	C	0110	6	80
1110	E	0111	7	90

REG29(1D): Current control_14 (0x63)

BIT	Name	Default	Description
7:5	IREF_CTRL_DA_50U<2:0>	011	Current Reference Control for TX driver amplifier
4:3	-	-	Reserved (Recognized as 0)
2:0	IREF_CTRL_VCO_100U<2:0>	011	Current Reference Control for TX VCO

Current control table

[Control coeds are represented by 4 bits including reserved bits. That is, 0 to 3 bit and 4 to 7bit are used to express each as 4bits.]

7 to 4 bit Code		3 to 0 bit Code		Current [uA]
BIN.	HEX.	BIN.	HEX.	
0000	0	0000	0	20
0010	2	0001	1	30
0100	4	0010	2	40
0110	6	0011	3	50
1000	8	0100	4	60
1010	A	0101	5	70
1100	C	0110	6	80
1110	E	0111	7	90

REG30(1E): BIN sweep range define_1 (0xC7)

BIT	Name	Default	Description
7:0	I_START_BIN<7:0>	1100 0111	Start BIN define of DLL MUX(199)

REG31(1F): BIN sweep range define_2 (0x00)

BIT	Name	Default	Description
7:0	I_STOP_BIN<7:0>	0000 0000	Stop BIN define of DLL MUX(0)

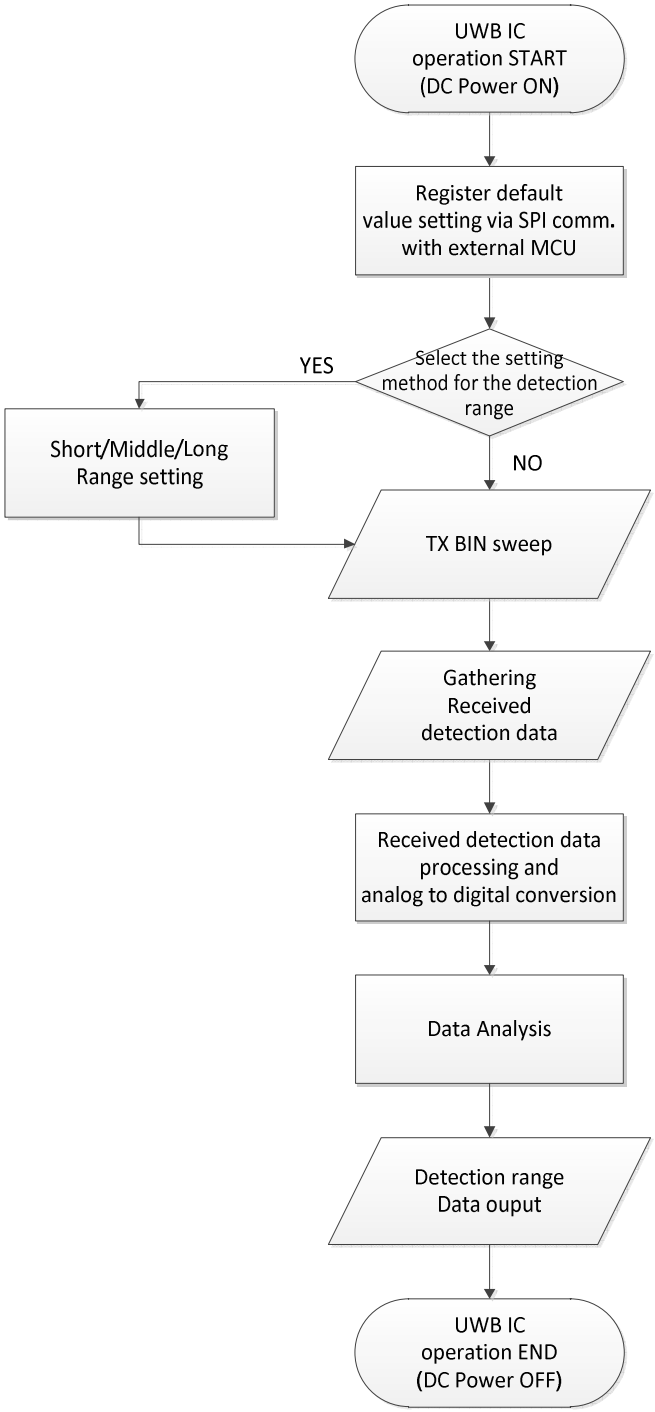
REG32(20): BIN sweep range define_3 (0xFF)

BIT	Name	Default	Description
7:0	I_HOLD_TIME<7:0>	1111 1111	Hold time define of DLL MUX(255)

REG33(21): Internal Timing logic (0x03)

BIT	Name	Default	Description
7	I_ENABLE		Enable for timing logic
6:2			
1	EN_SWEEP_TEST	1	H:External Bin Sweep Selection L:Logic Bin Sweep Test
0	EN_TX_CLK_TEST	1	H:TX_CLK_FROM_EXT L:TX_CLK_FROM_DLL Test

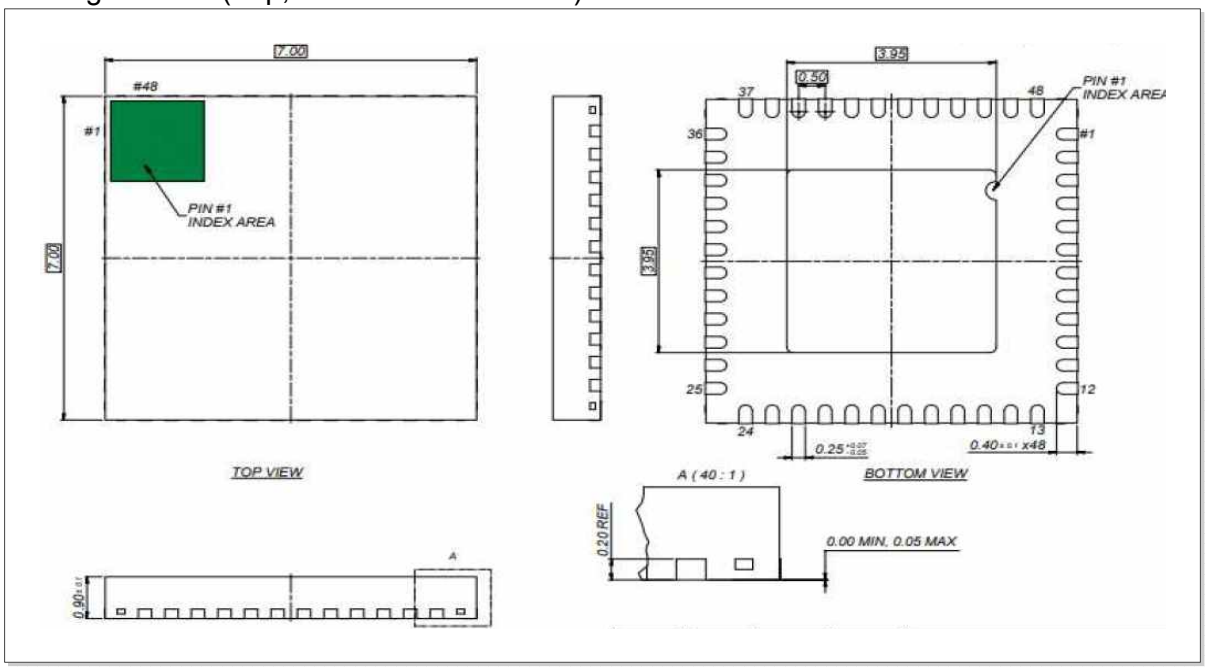
Register setting sequence



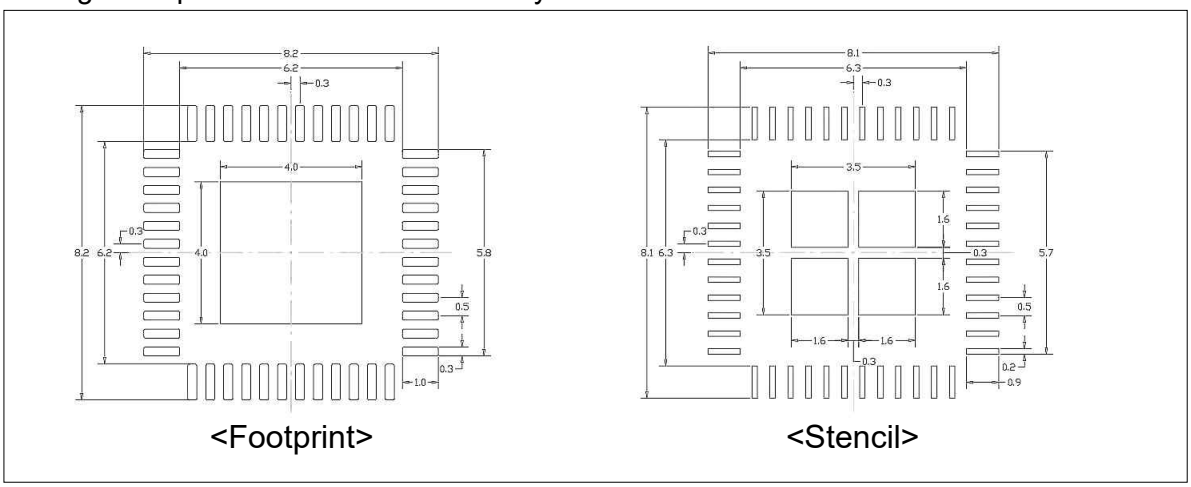
1. DC power (+1.2V, +3.3V) supply to the UWB IC
2. The default register values are set through SPI communication between the external control unit (ex. MCU) and UWB IC.
3. The User can select a setting method for the detection range.
   A. How to use the same setting for the whole detection range
      : Use the firmware source code or GUI to select this mode and set the receiving gain.
   B. How to distinguish the whole detection range by short/middle/long range.
      : Use the firmware source code or GUI to select this mode and set the range of short/middle/long range to BIN NO. And set the receiving gain according to each range using register 06~07.
4. TX BIN starts sweep and propagate Tx signal (External Tx antenna required)
5. Gathering received detection data (External Rx antenna required)
6. Extracts the distance information from the received data, and coverts the extracted analog data into a digital data.
7. Analyze the digitized signal on the external MCU.
8. Outputs information on the detection range of the object obtained through the UWB IC.
9. If the object detection is finished, turn off the power and end the operation.

Physical Dimension

- Package outline (Top, side and bottom view)



- Package Footprint and stencil for PCB Layout



<Footprint> <Stencil>

- IC Marking Layout